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10/562,235	10/31/2006	Syouji Nogami	P35795	8539

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EXAMINER	
MCCALL SHEPARD, SONYA D	
ART UNIT	PAPER NUMBER
2813	
MAIL DATE	DELIVERY MODE
02/23/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,235	NOGAMI ET AL.	
	Examiner	Art Unit	
	Sonya D. McCall-Shepard	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I claims 1 to 11, 13 and 14 in the reply filed on 20 April 2009 is acknowledged. The traversal is on the ground(s) that unity of invention requirements apply to this application and that examiner has not established a serious burden in the examination of the claims in a single application.

This is not found persuasive because the features common to these claims have been disclosed in JP 2003-218037 contained in Group I, claims 1 to 11, 13 and 14 and Group II, claims 12 and 15 to 24. There appear to be at least two special technical features contained in the above claims: (1) a method of manufacturing a semiconductor wafer and (2) a semiconductor wafer. These technical features appear to be present in various combinations (along with other features) in the above claims. Consequently, there are two inventions in the present application. The requirement of unity of invention is not satisfied *a posteriori*.

There would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply: (a) the inventions have acquired a separate status in the art in view of their different classification (Group I, claims 1 to 11, 13 and 14, class 438, method of making semiconductor devices and Group II, claims 12 and 15 to 24, class 257, semiconductor devices); (b) the inventions require a different field of search (Group I, claims 1 to 11, 13 and 14, class 438/478 and Group II, claims 12 and 15 to 24, class 257/347).

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1 to 11, 13 and 14 are rejected based on the Japanese Search Report document, JP 2003-218037.

4. Claims 1, 2, 4, 10 and 11 are rejected under 35 U.S.C. 102(a) as being anticipated by Nobuhiro et al. (JP 2003-218037).

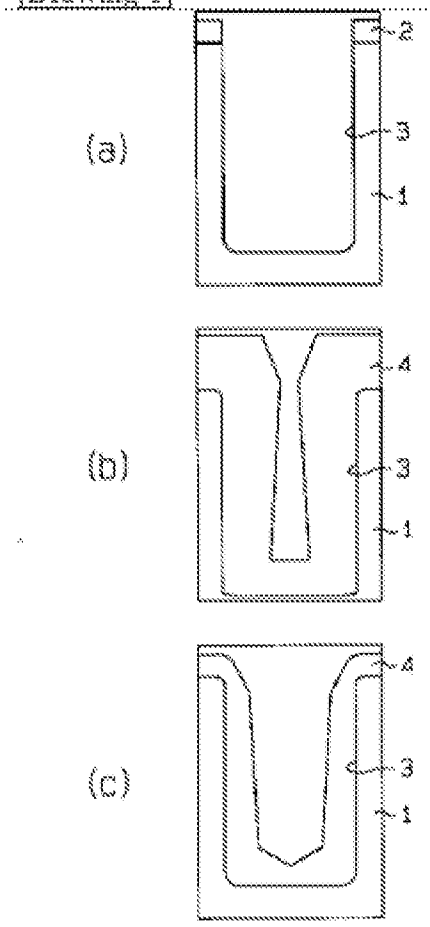
With regard to claim 1, Nobuhiro et al. disclose a manufacturing method of a semiconductor wafer comprising, wherein an epitaxial layer (4) is grown in a trench (3) of a semiconductor wafer (1) having a trench structure by gradually reducing a temperature in a temperature range of 400 to 1150°C or by gradually reducing a temperature and then lowering the temperature at a predetermined speed based on a vapor growth method while supplying a silane gas as a raw material gas, thereby filling the epitaxial layer in the trench (figs. 1-3, claims 1-10).

With regard to claims 2 and 4, Nobuhiro et al. disclose a step of forming a first layer (4) on an inner surface of the trench (3) of the semiconductor wafer (1) at a first temperature in the range of 900 to 1150°C by the vapor growth method; a step of forming a second layer (5) on a surface of the first layer (4) in the trench (3) at a second temperature in the range of 850 to 1100°C lower than the first temperature by the vapor growth method; and a step of forming a third layer (6) on a surface of the second layer (5) in the trench (3) at a third temperature in the range of 800 to 1050°C lower than the second temperature by the vapor growth method so that

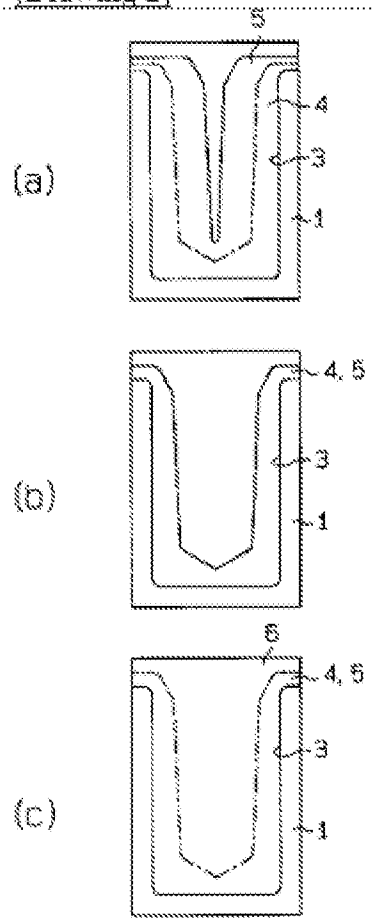
the epitaxial layer consisting of the first layer, the second layer and the third layer is filled in the trench (figs. 1-3, claims 1-10)

With regard to claims 10 and 11, Nobuhiro et al. disclose a temperature at which the epitaxial layer is grown by the vapor growth method falls within a range of 650 to 950°C (figs. 1-3, 8).

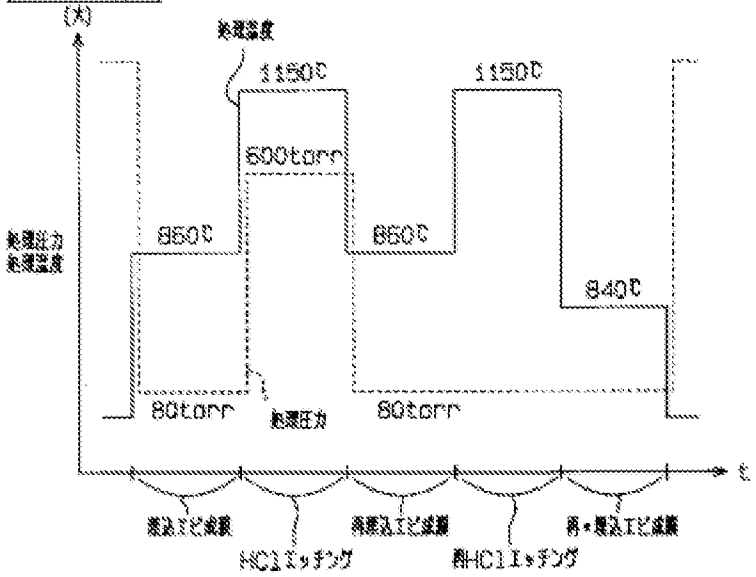
[Drawing 1]



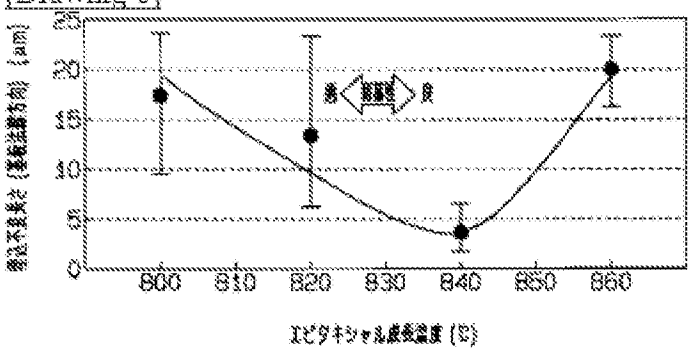
[Drawing 2]



[Drawing 3]



[Drawing 8]



Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 3, 5 and 6, 7, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nobuhiro et al. (JP 2003-218037).

With regard to claim 3, Nobuhiro et al. disclose a step of forming a first layer (4) on an inner surface of the trench (3) of the semiconductor wafer (1) at a first temperature in the range of 900 to 1150 °C by the vapor growth method; a step of forming a second layer (5) on a surface of the first layer (4) in the trench (3) at a second temperature in the range of 850 to 1100°C lower than the first temperature by the vapor growth method; a step of forming a third layer (6) on a surface of the second layer (5) in the trench (3) at a third temperature in the range of 800 to 1050°C lower than the second temperature by the vapor growth method (figs. 1-3). Nobuhiro teaches a step of repeating the layers one or more times (claim 2), therefore one having ordinary skill in the art at the time the invention was made would recognize that the repeating step of Nobuhiro, would be obvious in order to fill the trench with multiple layers for use in a semiconductor device. Nobuhiro et al. do not teach a step of forming a fourth layer on a surface of the third layer in the trench at a fourth temperature in the range of 750 to 1000°C lower than the third temperature by the vapor growth method so that the epitaxial layer. This is prima facie

obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious). One of ordinary skill in the art at the time of the invention would recognize that it would be obvious to optimize variables to achieve desired characteristics of semiconductor device.

With regard to claim 5, Nobuhiro et al. disclose a step of forming a first layer (4) on an inner surface of the trench (3) of the semiconductor wafer (1) at a first temperature in the range of 900 to 1150 °C by the vapor growth method; a step of forming a second layer (5) on a surface of the first layer (4) in the trench (3) at a second temperature in the range of 850 to 1100°C lower than the first temperature by the vapor growth method; a step of forming a third layer (6) on a surface of the second layer (5) in the trench (3) at a third temperature in the range of 800 to 1050°C lower than the second temperature by the vapor growth method (figs. 1-3). Nobuhiro et al. teach a step of repeating the layers one or more times (claim 2), therefore one having ordinary skill in the art at the time the invention was made would recognize that the repeating step of Nobuhiro et al., would be obvious in order to fill the trench with multiple layers for use in a semiconductor device. Nobuhiro et al. do not teach a step of forming a fourth layer on a surface of the third layer in the trench by the vapor growth method while reducing a temperature from

the third temperature at a speed of 1 to 100°C/min. This is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious). One of ordinary skill in the art at the time of the invention would recognize that it would be obvious to optimize variables to achieve desired characteristics of semiconductor device.

With regard to claims 6, 7, 13 and 14, Nobuhiro et al. do not explicitly teach the width of the layers with respect to the trench. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious). One of ordinary skill in the art at the time of the invention would recognize that it would be obvious to optimize variables to achieve desired characteristics of semiconductor device.

8. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nobuhiro et al. (JP 2003-218037) in view of Yamauchi et al. (US 6,495,294).

With regard to claim 8, Nobuhiro et al. teach a semiconductor wafer left in the air for eight hours or more in a state where a trench has been formed in the semiconductor wafer or in a state where the first layer, the second layer or the third layer has been formed on the inner surface of the trench. Nobuhiro et al. do not teach a semiconductor wafer is dipped in a mixture of an alkaline water solution and hydrogen peroxide solution having an etching rate of 0.1 to 1 nm/min for 1 to 10 minutes and cleansed, and then the semiconductor wafer is dipped in fluorinated acid for 0.1 to 60 minutes and cleansed. Yamauchi et al. teach a semiconductor wafer is dipped in an acidic or alkaline etchant to increase a width of the trench before forming the third layer or the fourth layer required to completely fill the inside of the trench of the semiconductor wafer and cleansed in HF (col. 9, lines 1-5, col. 18, lines 30-33). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a common etchant such as an alkaline water solution and hydrogen peroxide solution to increase a width of the trench before forming the third layer or the fourth layer required to completely fill the inside of the trench of the semiconductor wafer as taught by Yamauchi to improve the filling property. The above combination does not teach a solution having an etching rate of 0.1 to 1 nm/min for 1 to 10 minutes, nor dipping the semiconductor wafer fluorinated acid for 0.1 to 60 minutes, this is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in

degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious). One of ordinary skill in the art at the time of the invention would recognize that it would be obvious to optimize variables to achieve desired characteristics of semiconductor device.

With regard to claim 9, Nobuhiro et al. teach a semiconductor wafer etched to increase the width of the trenchin a gaseous environment before forming multiple layers after the first and second layers required to completely fill the inside of the trench of the semiconductor wafer (claim 2), but does not teach a semiconductor wafer is dipped in an acidic or alkaline etchant having an etching rate of 0.1 to 1 μm/min for 0.1 to 10 minutes to increase a width of the trench before forming the third layer or the fourth layer required to completely fill the inside of the trench of the semiconductor wafer. Yamauchi et al. teach a semiconductor wafer is dipped in an acidic or alkaline etchant to increase a width of the trench before forming the third layer or the fourth layer required to completely fill the inside of the trench of the semiconductor wafer (col. 9, lines 1-5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a common etchant such as an acidic etchant to increase a width of the trench before forming the third layer or the fourth layer required to completely fill the inside of the trench of the semiconductor wafer as taught by Yamauchi to improve the filling property. The above combination does not teach an etching rate of 0.1 to 1 μm/min for 0.1 to 10 minutes, this is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also

In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious). One of ordinary skill in the art at the time of the invention would recognize that it would be obvious to optimize variables to achieve desired characteristics of semiconductor device.

Response to Arguments

9. Applicant's arguments filed 17 November 2009 have been fully considered but they are not persuasive. The prior art of record discloses a manufacturing method of a semiconductor by gradually reducing the temperature in a temperature range of 400-1150°C or by gradually reducing the temperature and then lowering the temperature at a predetermined speed based on a vapor growth method while supplying a silane gas filling the epitaxial layer in the trench. Applicant does not recite that the starting temperature is 400°C nor the ending temperature is 1150°C, it is a range and the prior art of record shows a temperature at 860°C to 840°C, a gradual decrease in temperature (figs. 1-3, claims 1-10).

In addition, applicant has used the term "speed" in reducing the temperature however, the term should be "rate" because the flow of gas is a rate and not a speed as recited in claims and Figures 6 and 8. Applicant has also used a term "predetermined" and because the applicant has used this term it is highly suggested that this rate be disclosed (ie 10°C per minute or 5°C per second) a value that is supported by the specification since one of ordinary skill in the art at the

time the invention was made could not determine with any reasonable certainty that the claimed inventive steps is actually reproducible. Also the flow rate of the silane will also affect the predetermined flow rate (not the speed) as recited in the claims.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sonya D. McCall-Shepard whose telephone number is 571-272-9801. The examiner can normally be reached on Monday - Friday 8:30-5:00 E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Landau can be reached on 571-272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. D. M./
Examiner, Art Unit 2813

/W. David Coleman/
Primary Examiner, Art Unit 2823